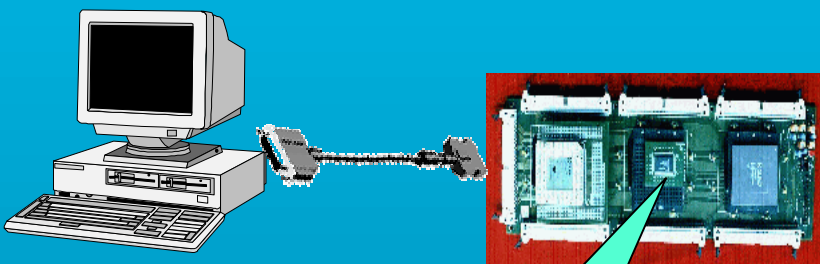


Asic Prototyping Board

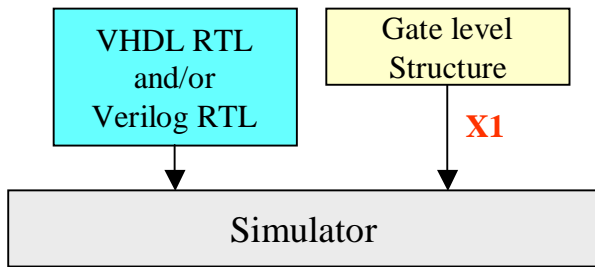
Asic Prototyping Board



Acceleration
Emulation
Validation

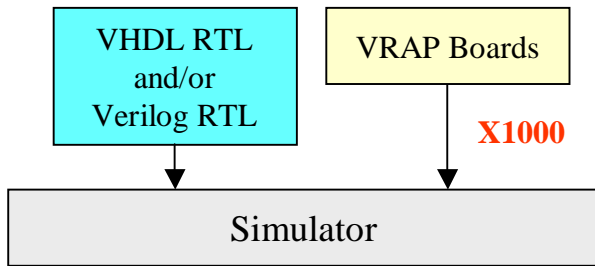
Asic Prototyping Boards linked with any VHDL/Verilog Simulator running on PC or WS Compilation/Simulation runs more than 1000 times Faster

VDesign, which is specialized in VHDL/FPGA Design has designed, developed, and manufactured a VRAP family Boards to Accelerate, Emulate and Validate any VHDL/Verilog design. The first board called **VRAP-AEB** (Acceleration, Emulation Board) is used to speed up the gate level simulation by a factor more than 1000 times faster than a software gate level simulation. This board is also used for ASIC emulation on the customer application board. See more detail in this brochure. The second board called **VRAP-UCB** (Universal Chip Board) is used to validate ASIC prototype or FPGA from any FPGA vendor. See more detail in this brochure. The VRAP family board includes a re-programmable board (Daughter board), a system software and utility programs and can be used for ASIC prototyping, FPGA validation, Co-Simulation Software and hardware, IP Netlist validation, SOC, regression test.



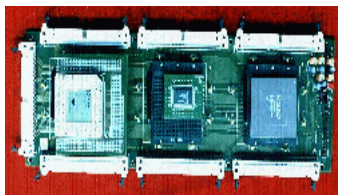
Traditional approach

Generally, the Engineer mix VHDL/Verilog RTL code and gate level structure in a same design. This approach can be used to simulate an IP netlist, or ASIC netlist and RTL code. If the simulation at the RTL level is enough fast, unfortunately the global simulation is relatively slow due to the gate level simulation.

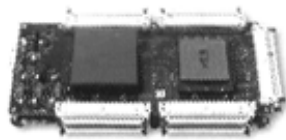


Using VRAP family boards

To address this problem, **VDesign** provides a hardware solution linked with any VHDL/Verilog simulator. The architecture at the gate level is fitted into VRAP family boards containing up to 18 million to 288 million (Using Cascade version) FPGA gates, the RTL architecture is simulated by the in built software. The gate level simulation is accelerated by a factor up to **1000**.

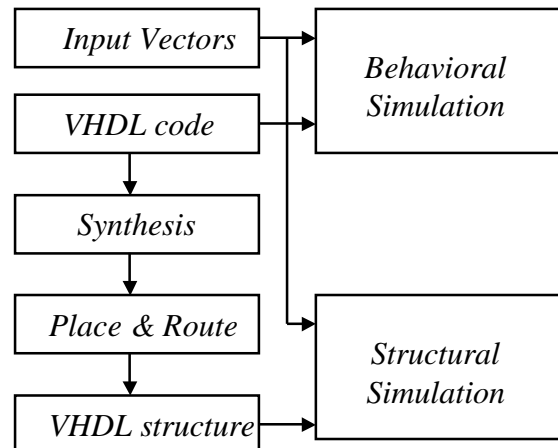


VRAP-AEB



VRAP-UCB

VRAP Family Boards



Design Flow for using VRAP Boards

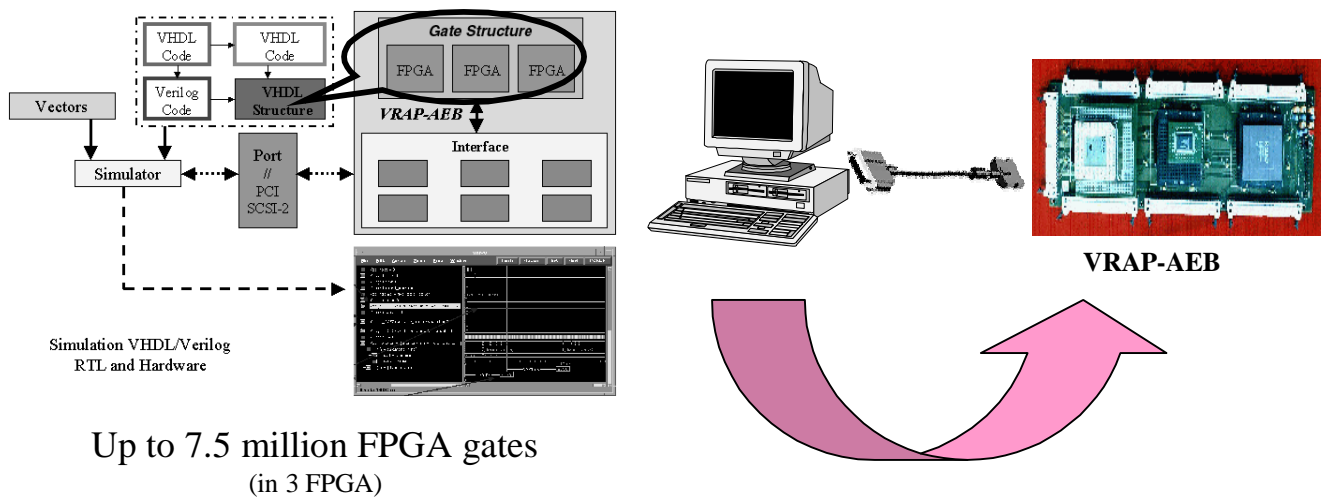
VRAP - AEB

Work with

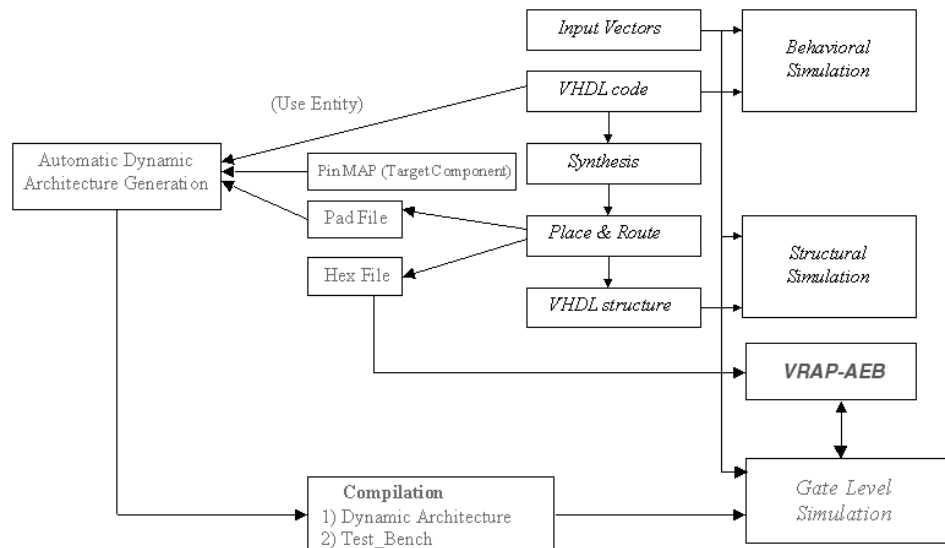
- PCI
- PC/Windows-95/98/NT/2000 and WS/Solaris
- Any VHDL/Verilog Simulator

Usage

- Functional Simulation Acceleration at the gate level
- Functional Simulation Acceleration of any IP Netlist
- ASIC Emulation on Customer Application Board



Methodology for using VRAP-AEB



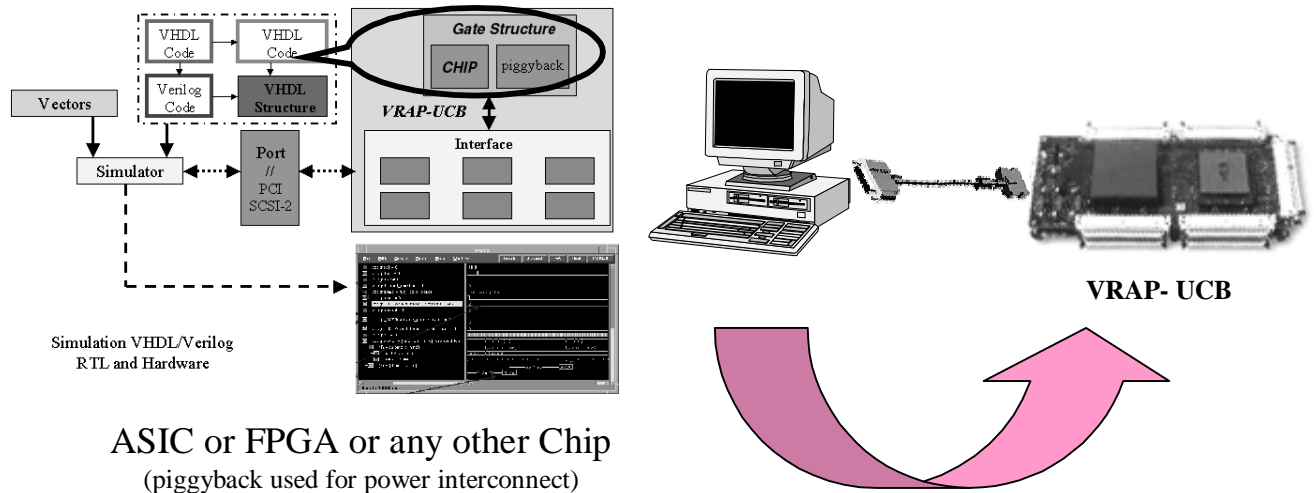
VRAP - UCB

Work with

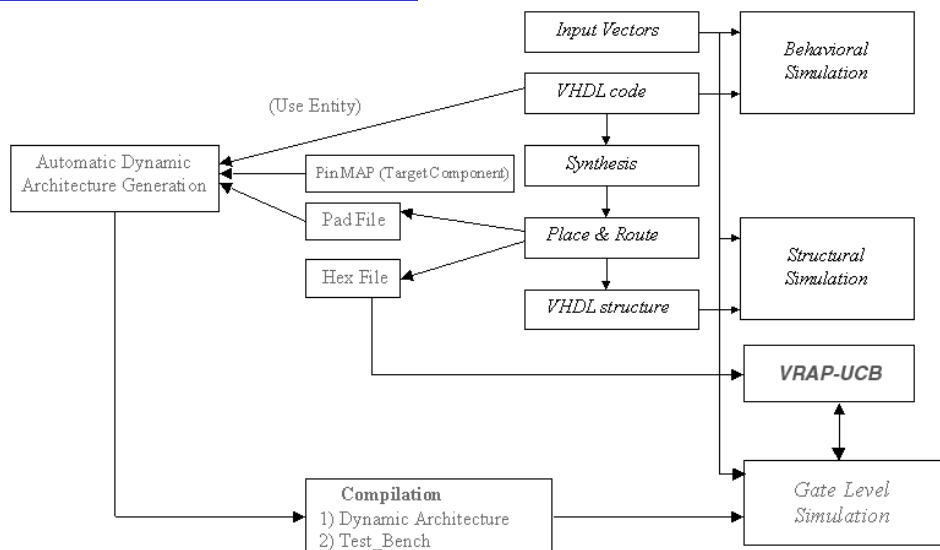
- PCI
- PC/Windows-95/98/NT/2000 and WS/Solaris
- Any VHDL/Verilog Simulator

Usage

- Simulation Acceleration at the gate level
- Simulation Acceleration of any IP Netlist
- Physical Chip used in your VHDL/Verilog Design
- ASIC prototype or FPGA validation
- Regression tests



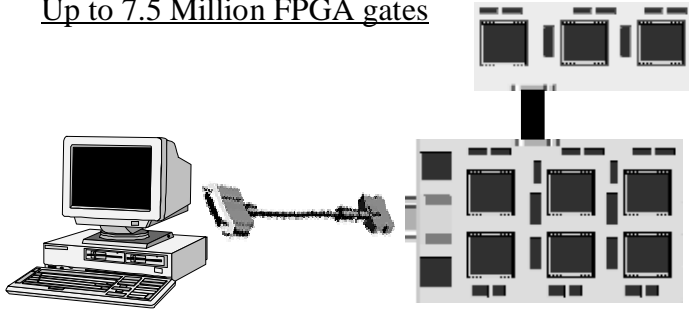
Methodology for using VRAP-UCB



Methodology for using VRAP family Boards

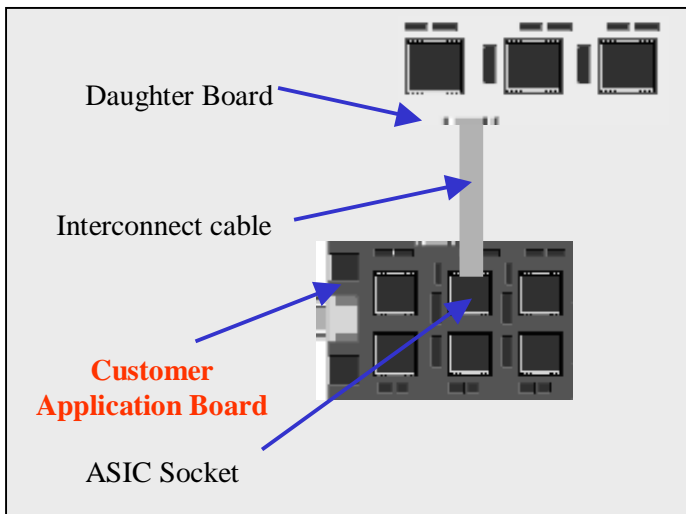
Step1 - Acceleration

Up to 7.5 Million FPGA gates



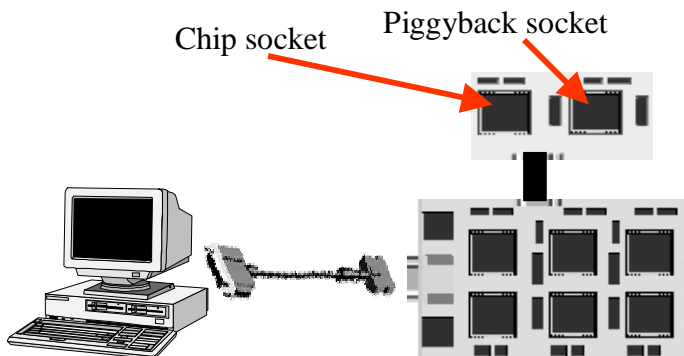
VRAP-AEB is used for a Functional simulation acceleration at the gate level. VRAP-AEB has 2 boards, a mother board that is used to interface the daughter board to the simulator. The daughter contain up to 7.5 million FPGA gates in 3 Chips. VRAP-AEB can be connected to any VHDL/Verilog Simulator available on the market. 299 I/O PIN are connected between Mother board and Daughter board.

Step2 - Emulation



As soon the Functional simulation is over, the daughter board can be used to emulate the ASIC prototype or IP netlist in his application board. To use this feature, the Engineer has to disconnect the daughter board from the mother board and connect the daughter board to the ASIC socket with the cable provided by **VDesign**. The picture shows the daughter board connected to the Application board .

Step3 - Validation

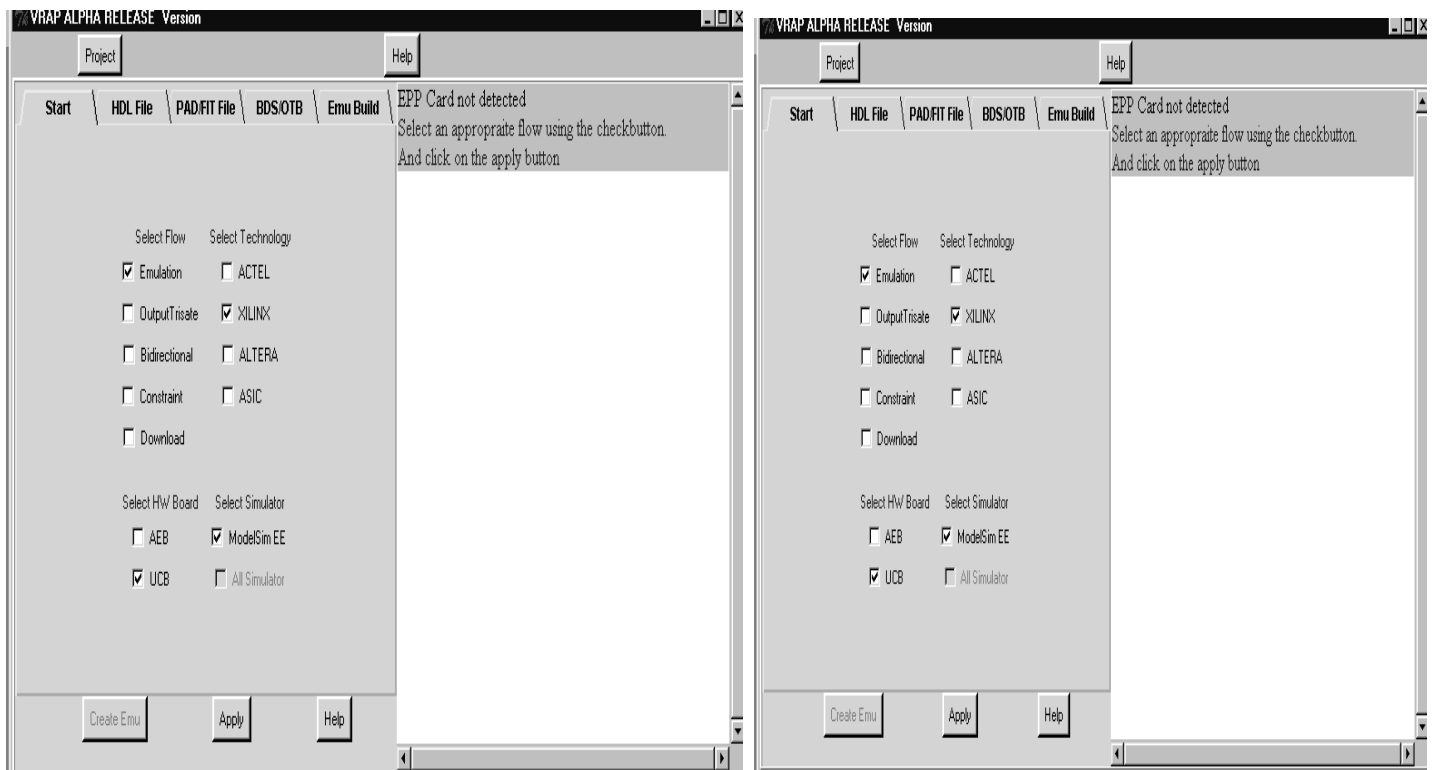


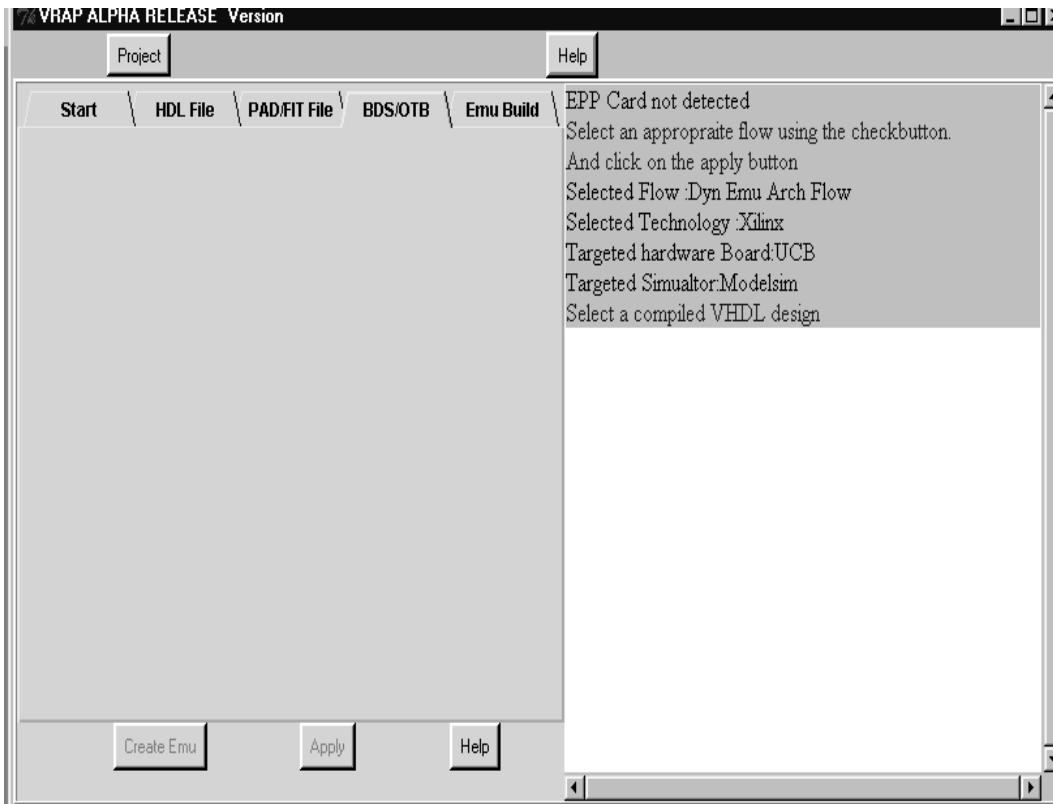
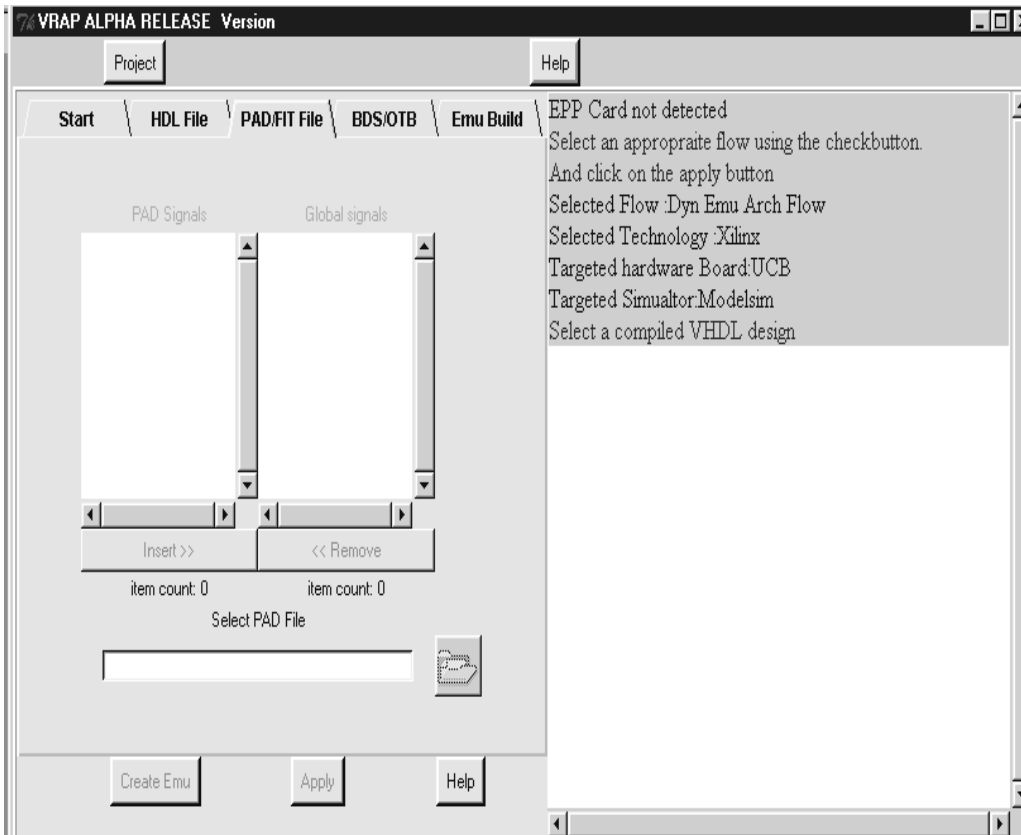
VRAP-UCB has two sockets, and it is used for ASIC or FPGA validation. The first one receive the CHIP, and the second one is used to interconnect the power to the chip. The Engineer can verify any ASIC or FPGA in using the same stimulus. The simulation provide all necessary Inputs to the chip and gets the result from the Chip. The VRAP-UCB board can receive any other chip, that can be integrated in any VHDL or Verilog design.

Specifications

VDesign Private Limited		
BOARD	VRAP-AEB	VRAP-UCB
Chip Used	Altera and Xilinx	FPGA from any vendor or ASIC Customer
Chip Power Supply	5v / 3,3v / 2,5v	1,8v / 2,5v / 3,3v / 5v (any three)
Number of FPGA gates	Up to 7.5 Million in 3 Chips	Unlimited
Number of I/O's	299	299
Package of Chip	Any package (Adapter provided for PGA)	Any package (Adapter provided for PGA)
Number of Chips on Board	3, Manual partitioning	1
WORKSTATION		
PC Platform	Available	Available
Sun WorkStation	Available	Available
INTERFACE		
Interface PC	Direct PCI	Direct PCI
Interface SUN	Direct PCI,	Direct PCI,
Operating System		
Operating System	Win 95/98/NT/2000	Win 95/98/NT/2000
Operating System	Solaris	Solaris
SIMULATORS Supported		
ModelSim/EE (MTI)	Available	Available
ModelSim/PE (MTI)	Available	Available
LeapFrog (Cadence)	Available (*)	Available (*)
Affirma (Cadence)	Available PC based	Available PC based
VisualHDL (Summit)	Available PC based	Available PC based
VSS (Synopsys)	Available (*)	Available (*)
ALDEC Simulator	Available PC based	Available PC based
Usage Purpose		
Behavioral Acceleration Simulation	No	No
Structural Acceleration Simulation	Functional only	Functional
Others Features		
Record all internal Signals	Available (*)	Available (*)
Timing	Available (*)	Available (*)
Comparison Behavioral/gate level	Available	Available
(*) Contact us for further details	(Acceleration Emulation Board)	(Universal Chip Board)

Utility Software





Performance Analysis

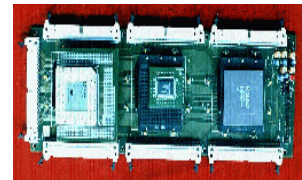
<i>DESIGN</i>	<i>VRAP</i>	<i>BEHAVIORAL</i>	<i>STRUCTURAL</i>	<i>% CLB</i>	<i>% IOs</i>	<i>Time saved</i>
	<i>Simulation</i>	<i>Simulation</i>	<i>Simulation</i>			
	In Minutes	In Minutes	In Minutes			In Minutes
Test Counter	4	89	2 400	66	16	2 396
Synchro	10	1	204	26	66	195
BY64	2	2	222	45	2	220
BlkAllPins	11	12	335	5	66	324
Counter32	4	1	12	1	15	8

Products Available On PC & Workstation

VRAP-AEB

For VHDL/Verilog Logic Simulation Acceleration at the gate level and ASIC Emulation

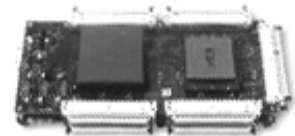
- Contains up to **7.5 to 18 Million** FPGA gates in 3 x FPGA
- Maximum of **299** I/O's
- Compilation **1000** times faster
- Simulation **1000** times faster
- Can mix Behavioral code and VRAP-AEB Board in a same design
- Comparison between behavioral simulation and VRAP-AEB
- Up to 16 systems can be cascaded. Un limited cascade using HUB



VRAP-UCB

For VHDL/Verilog Logic Simulation Acceleration at the gate level and FPGA/ASIC Validation

- Supports all major FPGA from FPGA vendors
- Maximum of **299** I/O's
- Compilation **1000** times faster
- Simulation **1000** times faster
- Can mix Behavioral code and VRAP-UCB Board in a same design
- Comparison between behavioral simulation and VRAP-UCB
- Up to 16 Systems can be cascaded .Un limited cascade using HUB.



VDesign Activities

- IP cores development
- Feasibility studies
- Implementation oriented specification works
- Exploration of Architecture alternatives
- VHDL Coding, Simulation and Synthesis
- Incorporation tests - Boundary Scan, JTAG
- FPGA Prototyping - VDesign supports Major FPGA Vendors

Services of VDesign help you Synthesize, Place & Route, Validate and finish your project successfully

VDesign

www.vdesignpl.com

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