VRAP-UCB

(VDesign Rapid ASIC Prototyping - Universal Chip Board)

APPLICATION NOTE

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Today we are challenged to produce the quality product at low cost and gain early entry into the market. Be it be Electronic systems, Components, ip cores, fast time to market is the mantra in this domain.

Given a specification, the task of the designer is to implement the design in FPGA's / ASIC. The designers spend much of their time to validate their specification than coding. System level simulations demand excessive computer time and need to validate each and every case.

VDesign has come up with a novel and a low cost product VRAP-UCB (universal chip board) using "open interconnect platform" to allow the designers to do functional verification of design as easy as IC testing. The hardware platform (VRAP-UCB) with socket for 299 I/O's is coupled to the software simulator.

Any design or modules of a design can be targeted to a FPGA and the module's input and output are coupled to the software simulator. Simulator can run some portion of the behavioral code in the PC and can interact with the VRAP-UCB.

This speeds up the verification of corner cases and regression test. Engineers save lot of time in testing the cores.

The applications are multitude in nature.

1. Single CHIP Emulation on to any target technology using ONE VRAP-UCB:

   The FPGA /ASIC custom or IP developer can target the design on to the largest density FPGA from any vendor available in the market, using the VRAP-UCB. Normally, based on statistics,

for every 4 ASIC gates, equivalent is one FPGA gate. Based on their design the user can choose the best BASIC BUILDING BLOCKS from any device family of XILINX, ALTERA, or any other vendor. The VRAP-UCB supports up to 299 I/O's, and each pin can be individually configured as INPUT, OUTPUT or INOUT. More I/O's are supported in the future versions of the product. Today, one can use the available **2.5 Million gate FPGA** from the market.

2. MULTI CHIP Emulation on to same or different target Technology using more than ONE VRAP-UCB:

   Incase the design has more than one block in the top design, and if each module can be fitted into the largest available single chip FPGA, then each block can be separately targeted onto the different VRAP-UCB. This allows the flexibility for the designer to **avoid manual partitioning.**

   Cascading more VRAP-UCB systems can be done through HUBs. By using 8 VRAP-UCB systems, amounting to **20 (2.5*8) Million gate design**.

3. Acceleration by hardware :

   Emulation using FPGA'S accelerates the simulation by an order of **more than 1000 times** compared with simulation on the PC's. Also since there is no density limitation, the acceleration speed increases exponentially with higher gate counts. The system speed is limited only by the transfer bandwidth of the vectors.

4. Validation of any specific **CHIP / IP**:

   When the Chip (ASIC) has arrived from the foundry, the functional verification of the chip can be done and **compared with the behavioral results.** Another way is to emulate the design using FPGA on the first VRAP-UCB and compare it

with the ASIC on the second VRAP-UCB. This method allows us to **compare with PHYSICAL CHIPS.** This method allows the IP developers to validate their code with existing Standard part components or ASIC.

5. Integration with Multi Chip / Multi Technology:

   Designs having multiple FPGA's can be individually mounted on to different VRAP-UCB systems.
   For ex, one can ***mix multiple technologies*** also.

6. Integration with **Hard IP** cores.

   The Designers can download only the hex files of the IP (FPGA) cores specific to any FPGA device from the IP warehouse for evaluation purpose. The Designers can build systems by adding the HARD IP as a black box in his design and can do the simulation.

7. Test Bench generation from microprocessors or any ASSP:

   Designers who wish to build peripheral devices around any microprocessor can simply ***buy off the shelf component*** from the market and insert it in VRAP-UCB using suitable adaptors. The only criteria being that the processor should be CMOS and STATIC. The designer ***does not need to buy expensive BUS functional model*** of the microprocessor. The user can build a simple ICE (In Circuit Emulator) using VHDL code or VDesign can develop it for the customer.

8. Any standard Interface with ASSP (Static CMOS, CPLD, FPGA, PLD, ASIC, Memories):

   It goes without saying that one can ***interface his code with any standard*** ASSP (Application Specific Standard Part). This includes ***microprocessors, microcontrollers and DSP's also.***

The device should be static in nature.

9. Specification validation:

One can validate his specification and do regression test much faster by using these low cost VRAP-UCB's.

10. Any package / adaptor support:

The following pacakges are available.
QFP, PLCC, PGA, BGA.
Other packages can be supported on request .

11. ASIC design Considerations:

a) Multi clock support
If the design uses GATED clocks or special ClOCK generation circuit, or multiple clocks , FPGA allows to route the internal clock node as GLOBAL signal throughout design within the FPGA.
b) Multi partitioning using modules less than 300 I/O's.

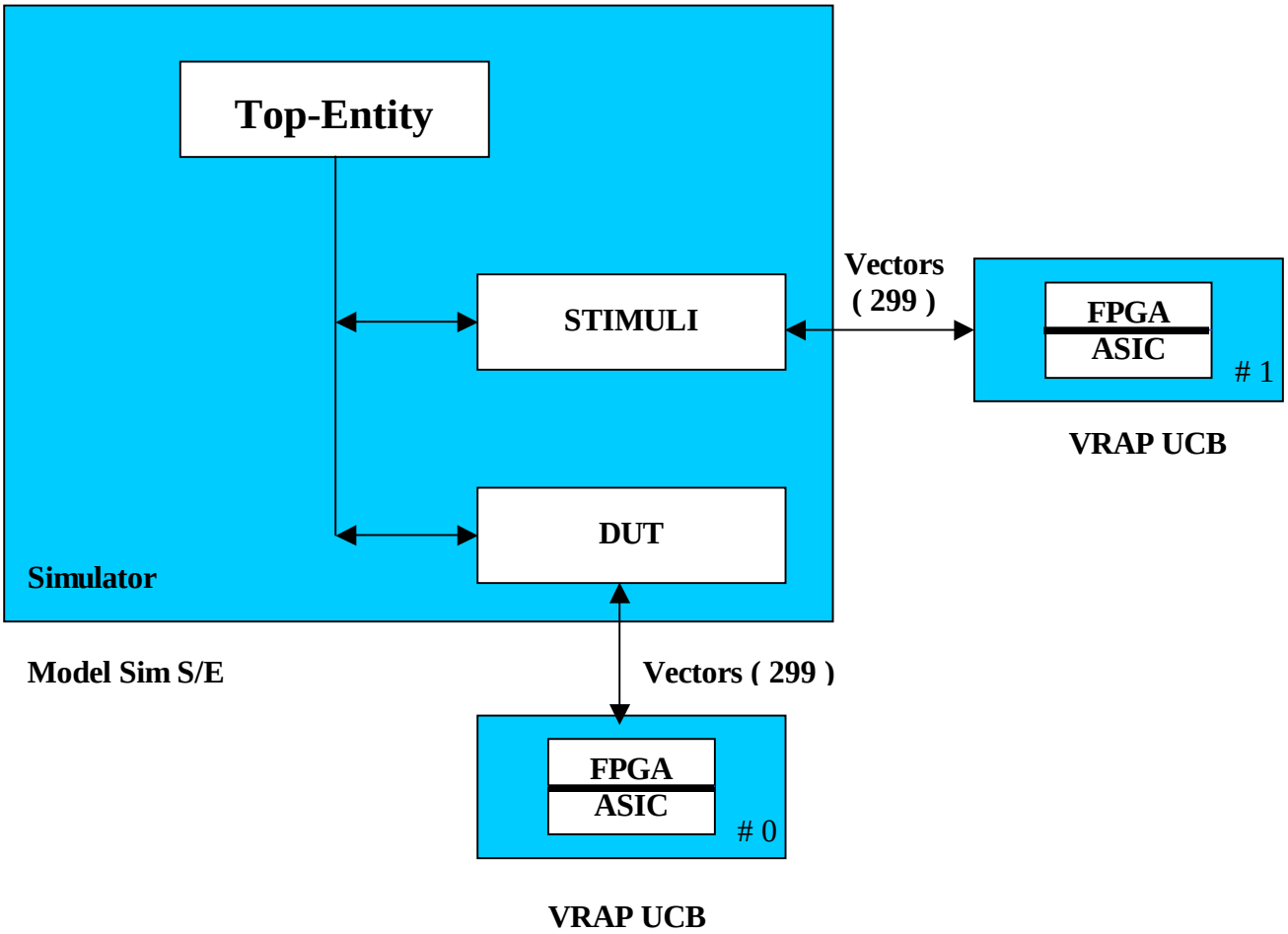
12. Memory Support :

Static Rams can be plugged on to UCB using suitable adaptors. For large memory support, we can provide SDRAM modules, which can be accessed like a simple SRAM. File I/O's can be mapped on to these memories. Real time samples obtained from capture cards can be loaded into these large SDRAM's. These reduces the hard disk access time, which drastically **reduces the system simulation time.**

SYSTEM ARCHITECTURE

Let us have a look at the architecture of the VRAP-UCB. Assume you have two modules at top level, i.e. one is STIMULI and the other is the DUT (Device Under Test). The DUT can now be synthesized and routed for a particular technology and the HEX file obtained can be downloaded into the VRAP-UCB board. If the "STIMULI" is synthesizable, than all the good, that it can also be downloaded into another VRAP-UCB board. Run the simulator and watch the results on the screen. You can really feel the performance difference in using VRAP-UCB than the software simulator.

SOFTWARE VIEW



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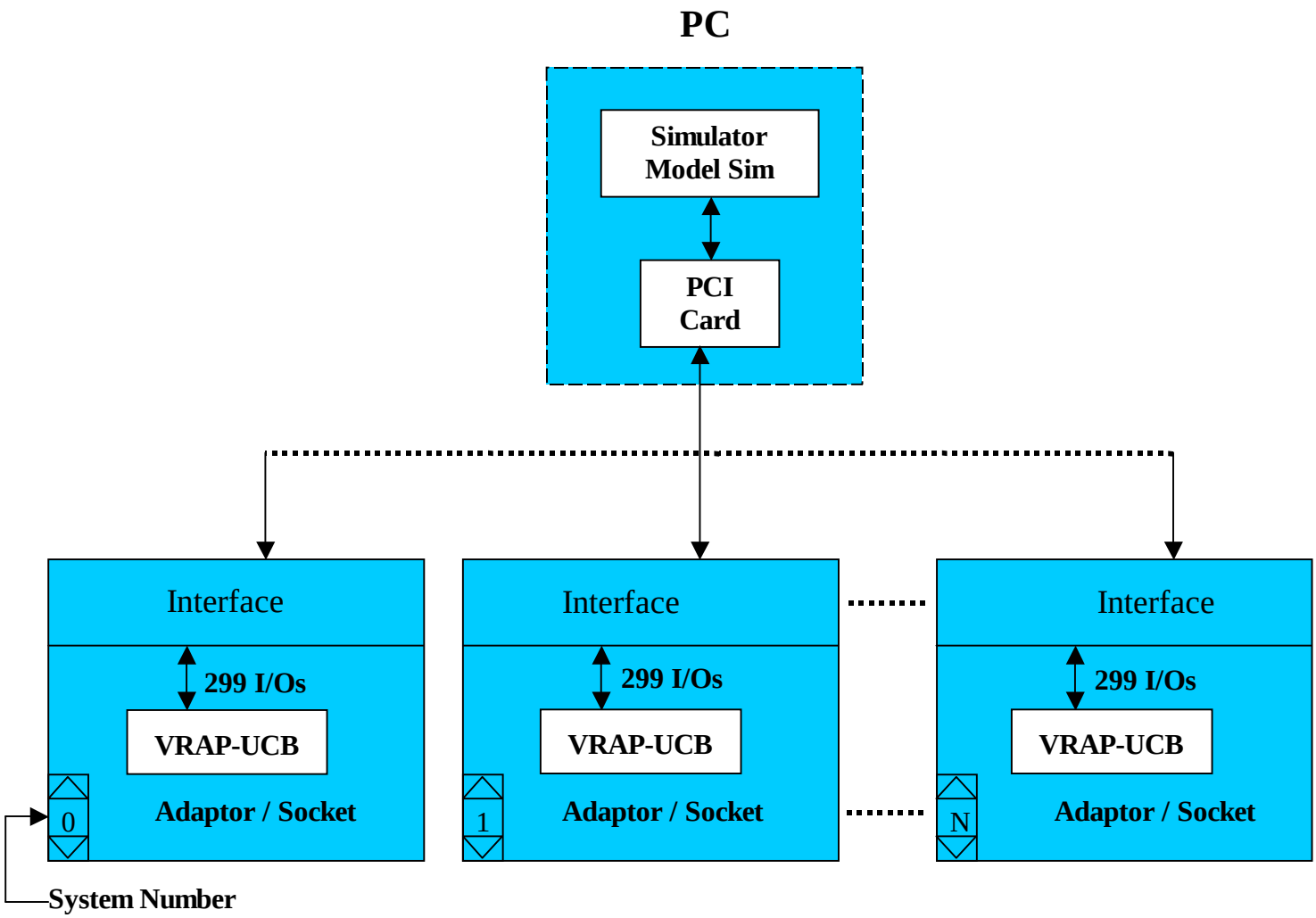
HARDWARE VIEW



N: Depends on using HUB or without HUB

- Multiple VRAP-UCBs can be cascaded using HUBs.
- Maximum I/Os in each VRAP-UCB: 299.
- PIGGYBACK is required to configure the power pins of FPGA or any CHIP.

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Please contact us for any particular certification pertinent to your country.
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