



VRAP-AEB

(VDesign Rapid Asic Prototyping - Acceleration Emulation Board)

HIGHLIGHTS

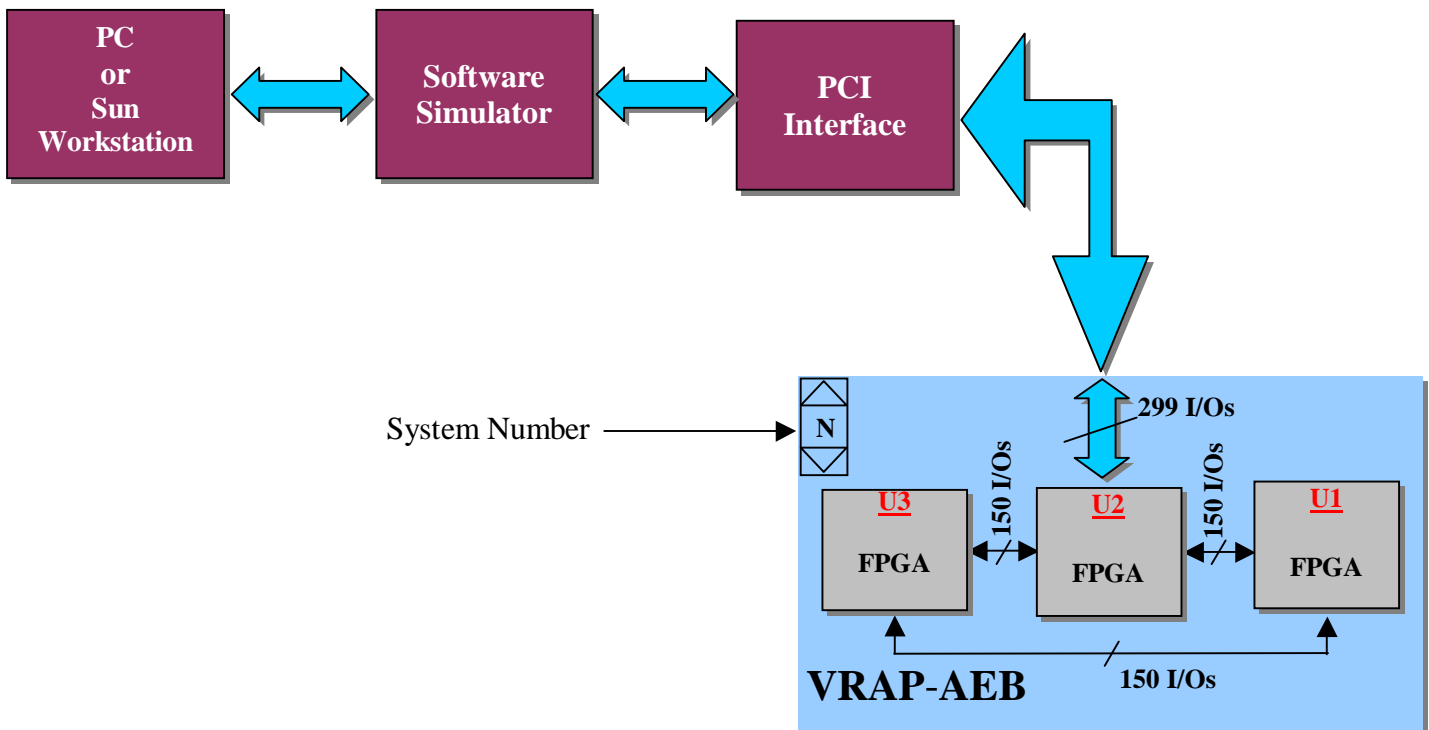
- ❑ Three Chip Emulation using FPGA.
- ❑ Support for Xilinx Virtex, Virtex2 family or Altera APEX or other FPGA's.
- ❑ Universal Daughter Board with 3 ZIF sockets.
- ❑ Upgradable with new High Density devices by changing only the adaptors and not the platform. Ensures life for the product.
- ❑ VHDL support for MODELSIM EE/SE.
- ❑ VERILOG Support for any Simulator using PLI.
- ❑ Number of I/O's per CHIP is 450.
- ❑ Number of I/O's per Board is 299.
- ❑ Several VRAP-AEB units can be cascaded*.
- ❑ Mix VRAP-AEB and VRAP-UCB in the same design.
- ❑ VRAP-UCB can be upgraded to VRAP-AEB.
- ❑ With Suitable adaptors, can be plugged on to your application board.
- ❑ Currently available 2.5Million x 3: 7.5million Gate.
- ❑ Adaptors come with BGA sockets for upgrading to better chips.



FEATURES

- ❑ Supports all major FPGA from major FPGA vendors.
- ❑ Maximum of 299 Board I/O's.
- ❑ Compilation is more than 1000 times faster.
- ❑ Simulation is more than 1000 times faster.
- ❑ Can mix behavioral code and VRAP-AEB board in the same design.
- ❑ Can compare between behavioral simulation and VRAP-AEB.
- ❑ Internal node monitoring is possible.
- ❑ Multiple VRAP' s can be cascaded*.
- ❑ Comes with VRAP PCI interface card from VDesign.
- ❑ Works with PC/Windows 9X, NT and Sun Sparc Workstation
(Solaris 2.6, 7 and 8).

BLOCK DIAGRAM





VRAP – AEB Ordering Information

CODE : VDVRAP – A – 3v3/5v – PC/WS – M/T – S/C – VH/VE/VV – HU01/02

Voltage Support :
 3v3: 3.3v, 3.3v, 2.5v/1.8v
 5v : 5v,3.3v,2.5v/1.8v

Operating System Support :
 PC: WIN9x, NT
 WS: Workstation
 (Sun Solaris 2.6,7 and 8 only)

Simulator Support :
 M : Model SIM SE/EE
 T : Other Simulators*

Unit Support :
 S : Singel Unit
 C : Cascadable Unit*

HDL Support :
 VH : VHDL only
 VE : Verilog only
 VV : Verilog,VHDL

HUB Support :
 HU01 : Without HUB
 HU02 : HUBs

*Contact Factory



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Release Version: Ver2.0, August 2001.